WHAT IS CLAIMED IS:

1. A test emulator for emulating a test apparatus comprising a plurality of test modules for supplying a test signal to devices under test respectively, comprising:

a plurality of test module emulation sections for emulating the plurality of test modules generating the test signal based on different cycles;

a control emulation section for emulating a control apparatus for controlling the test of the devices under test;

a synchronous emulation section for generating test signal generating timings, at which each of said plurality of test module emulation sections is to generate the test signal in simulation corresponding to cycle time of said test module emulation section, based on instructions from said control emulation section;

a timing alignment section for aligning the plurality of test signal generating timings generated by said synchronous emulation section in order of time, and outputting them one by one; and

a schedule section for causing said test module emulation section corresponding to one of the test signal generating timings output by said timing alignment section to generate the test signal in simulation in the cycle time corresponding to the test signal generating timing.

2. The test emulator as claimed in claim 1, further comprising a device under test simulating section for simulating operation of a device under test based on the test signal generated in simulation.

3. The test emulator as claimed in claim 1, wherein

said synchronous emulation section further generates interruption collection timings for collecting interruption to the control apparatus generated in simulation by each of said plurality of test module emulation sections during the generation of the test signal in the cycle time corresponding to the test signal generating timings,

said timing alignment section aligns the plurality of test signal generating timings and the plurality of interruption collection timings in order of time, and outputs

them one by one, and

said schedule section causes said test module emulation section corresponding to the interruption collection timing to notify said control emulation section of the interruption generated in simulation in the cycle time at which said test module emulation section generates the test signal just before the interruption collection timing, in case that said timing alignment section outputs one of the interruption collection timings.

4. The test emulator as claimed in claim 1, wherein

each of said plurality of test module emulation sections generates change timing of the test signal in the cycle time at the generation of the test signal in the cycle time corresponding to the test signal generating timing, and

the test emulator further comprises a DUT connection section for acquiring the plurality of change timings generated by said plurality of test module emulation sections, and for changing the test signal in simulation one by one in order of time based on the plurality of change timings.

5. The test emulator as claimed in claim 4, wherein

said DUT connection section supplies the plurality of change timings acquired from said plurality of test module emulation sections to said timing alignment section,

said timing alignment section aligns the plurality of change timings, the plurality of test signal generating timings, and the plurality of interruption collection timings in order of time, and outputs them one by one, and

said schedule section causes said DUT connection section to change the test signal in simulation at the change timing, in case that said timing alignment section outputs one of the change timings.

6. The test emulator as claimed in claim 1, wherein

each of said plurality of said test module emulation sections notifies said synchronous emulation section of the cycle end timing at which the cycle time ends during the generation of the test signal in the cycle time corresponding to the test signal

generating timing, and

said synchronous emulation section generates the test signal generating timings at which said test module emulation section generates the test signal in simulation corresponding to next cycle time based on the cycle end timing notified from each of said plurality of test module emulation sections.

7. The test emulator as claimed in claim 6, wherein said schedule section causes the interruption generated in simulation by said test module emulation section corresponding to the test signal generating timing to be notified to said control emulation section during the generation of the test signal in the cycle time just before the test signal generating timing, in case that said timing alignment section outputs the test signal generating timing corresponding to the next cycle time.

8. The test emulator as claimed in claim 1, wherein

each of said plurality of test module emulation sections is realized by operating test module emulation program corresponding to said test module emulation section by a computer, and the test module emulation program comprises:

a plurality of hardware emulation functions, being provided corresponding to a plurality of commands received by the test module from said control apparatus respectively, for emulating operation of the test module corresponding to the command; and

a control function used in order for said schedule section to cause the test emulator to generate the test signal in the cycle time corresponding to the test signal generating timing.

9. A record medium storing therein program for causing a computer to function as a test emulator for emulating test apparatuses comprising a plurality of test modules for supplying test signal to devices under test respectively, wherein the program causes the computer to function as:

a plurality of test module emulation sections for emulating the plurality of test modules generating the test signal based on different cycles;

a control emulation section for emulating a control apparatus for controlling the test of the devices under test;

a synchronous emulation section for generating test signal generating timings, at which each of said plurality of test module emulation sections is to generate the test signal in simulation corresponding to cycle time of said test module emulation section, based on instructions from said control emulation section;

a timing alignment section for aligning the plurality of test signal generating timings generated by said synchronous emulation section in order of time, and outputting them one by one; and

a schedule section for causing said test module emulation section corresponding to one of the test signal generating timings output by said timing alignment section to generate the test signal in simulation in the cycle time corresponding to the test signal generating timing.

10. A test module emulator for emulating a test module among a plurality of test modules by a test emulator for emulating test apparatuses comprising the plurality of test modules for supplying test signal to devices under test respectively based on a different cycle, wherein the test emulator comprises:

a control emulation section for emulating a control apparatus for controlling the test of the devices under test;

a synchronous emulation section for generating test signal generating timings, at which each of said plurality of test module emulation sections is to generate the test signal in simulation corresponding to cycle time of said test module emulation section, based on instructions from said control emulation section;

a timing alignment section for aligning the plurality of test signal generating timings generated by said synchronous emulation section in order of time, and outputting them one by one; and

a schedule section for causing said test module emulation section corresponding to one of the test signal generating timings output by said timing alignment section to generate the test signal in simulation in the cycle time corresponding to the test signal generating timing, and

the test module emulator comprises a pattern generator emulation section for generating the test signal in simulation in the cycle time corresponding to one of the test signal generating timings based on instructions from said schedule section.

11. The test module emulator as claimed in claim 10, further comprising a test module interface emulation section for notifying a synchronous emulation section of cycle end timing at which the cycle corresponding to one of the test signal generating timings ends, and causing said synchronous emulation section to further generate the test signal generating timing at which the test module emulator is to generate the test signal in simulation for the next time based on the cycle end timing.

12. A record medium storing therein program for causing a computer to function as a test module emulator for emulating a test module among a plurality of test modules as for a test emulator for emulating test apparatuses comprising the plurality of test modules for supplying test signal to devices under test respectively based on a different cycle, wherein the test emulator comprises:

a control emulation section for emulating a control apparatus for controlling the test of the devices under test;

a synchronous emulation section for generating test signal generating timings, at which each of said plurality of test module emulation sections is to generate the test signal in simulation corresponding to cycle time of said test module emulation section, based on instructions from said control emulation section;

a timing alignment section for aligning the plurality of test signal generating timings generated by said synchronous emulation section in order of time, and outputting them one by one; and

a schedule section for causing said test module emulation section corresponding to one of the test signal generating timings output by said timing alignment section to generate the test signal in simulation in the cycle time corresponding to the test signal generating timing, and

the program causes the computer to function as a pattern generator emulation section for generating the test signal in simulation in the cycle time corresponding to

one of the test signal generating timings based on instructions from said schedule section.

13. A test apparatus comprising a test module for supplying a test signal to a device under test, comprising:

a control apparatus for controlling a test of the device under test;

a test module for generating a test signal based on a cycle; and

a test module emulation section for emulating said test module, wherein

said control apparatus inputs an instruction about which of a real test or a simulation test is to be selected for the test of the device under test,

said control apparatus supplies said test module with a test program for testing the device under test and causes said test module to test the device under test when the instruction indicates that the real test of the device under test is to be performed, and

said control apparatus supplies said test module emulation section with a test program for testing the device under test and causes said test module emulation section to simulate the test of the device under test when the instructions indicates that the simulation test of the device under test is to be performed.

14. The test apparatus as claimed in claim 13, wherein

said control unit executes communication software for performing communication processing between said control unit and said test module, and

said communication software decides whether the test program is to be supplied to said test module or said test module emulation section based on the instructions included in calling for initializing the communication software in cooperation with said control apparatus.

15. A test emulator for emulating a test apparatus comprising a plurality of test modules for supplying a test signal to devices under test, comprising:

a plurality of test module emulation sections for emulating the plurality of test modules generating the test signal based on a cycle;

a control emulation section for emulating a control apparatus for controlling the

test of the devices under test; and

a schedule section for scheduling test signal generating timing at which each of said plurality of test module emulation sections is to generate test signal corresponding to a cycle time in simulation, wherein

said test module emulation section outputs variation of voltage of the test signal during the cycle time corresponding to the test signal generating timing by calling voltage setting method of an output channel object which emulates an output channel for multiple times on receiving the test signal generating timing by a function call, and

said test module emulation section notifies that output of the variation of the voltage of the test signal corresponding to the cycle time is finished by calling an end method of the output channel object output after the output of the variation of the voltage of the test signal corresponding to the cycle time is finished.

16. The test emulator as claimed in claim 15, wherein

said schedule section calculates a period during which all of said test module emulation sections finishes the output of the variation of the voltage of the test signal based on the end method notified from each of said plurality of test module emulation sections, and

the test emulator further comprises a device under test simulating section for acquiring the test signal within the period and simulates operation of the device under test during the period based on the test signal.

17. The test emulator as claimed in claim 15, wherein the output channel object forbids the variation of the voltage in the period during which the output of the variation of the voltage of the test signal was finished, which was notified by the end method, after the end method was called.